IN THE UNITED STATES PATENT & TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl. No.	:	10/803,464
Applicants	:	Noquil, et. al.
Filed	:	March 18, 2004 Art Unit: 2826
Title	:	MULTI-FLIP CHIP ON LEAD FRAME ON OVER MOLDED IC PACKAGE AND METHOD OF ASSEMBLY
Examiner	:	Tuan Quach
Docket No.	:	3016271 US01
Customer No.	:	44,331

Mail Stop: Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

DEAR SIR:

Further to the Notice of Appeal filed on February 28, 2006 in the above referenced case, Appellant hereby submits this Appeal Brief having a filing deadline of April 28, 2006.

TABLE OF CONTENTS

REAL PARTY IN INTEREST

The real party in interest is Fairchild Semiconductor Corporation, having a place of business in the city of South Portland, in the State of Maine, United States of America.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1 – 6 and 9 – 15 are pending in the application, Claims 1 – 6 and 9 – 15 are rejected, and Claims 1 – 6 and 9 – 15 are hereby appealed.

STATUS OF AMENDMENTS

The Appellant's response to the Final Office Action filed on February 27, 2006 sought to amend the claims subsequent to final rejection. This amendment was not entered by the Examiner per his Advisory Action of April 17, 2006.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention provides a multichip semiconductor package and packaging method that has two or more dies in a module where the dies are mounted on a lead frame and connected to external leads using different types of connections. One die is connected to the leads with wire bonding and the other die is connection with flip chip bonding. The prior art fails to show or suggest using different bonding structures on different dies that are placed in a common package. Instead, the prior art uses the same bonding technique for all dies in a package. The invention provides a surface mounted multichip module package that houses an integrated circuit for controlling one or more power MOSFETs that are also included in the package.

The package uses a leadframe having a die pad with upper and lower surfaces and a plurality of outer leads surrounding the die pad. The leadframe 10 of FIG. 1 holds a controller integrated circuit on one side and high and low side MOSFETs on the other side to provide a multichip module with logic and power devices. The leadframe 10 has source pads 24, 26 for receiving source studs and inner leads 34, 36 for receiving the gate studs. The inner source pads 24, 26 are integral with outer source leads 124, 126 respectively, for connecting the sources of the MOSFETs to the outer leads. The inner gate leads 34, 36 are integral with outer gate leads 134, 136, respectively. The outer leads receive ball contacts that may be attached directly to a printed circuit board. The outer gate leads 134, 136 are connected to the controller chip through wire bonds on the other side of the lead frame. The upper side of the lead frame with the integrated circuit is encapsulated in plastic insulating resin.

The invention is made by following the process steps shown in FIGS. 1 - 12. In FIG. 1 a single leadframe 10 is shown with its half etched MOSFET side facing the viewer. The leadframe 10 is carried on a tape 8 that has a number of leadframes. Each half etched leadframe has outer leads along opposite sides 2, 6. The leadframe has MOSFET source contact inner pads 24, 26 and gate inner leads 34, 36. As shown in FIG. 2, the MOSFET side of the leadframe is on the tape 8 and the controller side of the leadframe is exposed. A controller integrated circuit die 14 is placed on the controller side. Next, wire bonds 16 are applied to the die 14. Following wire bonding, the die 14 is molded over with plastic insulating material. See FIGS. 5, 6 and 26A-C. The molded dies 14 are removed from the mold and the molded package 10 is flipped onto its opposite side. Tape 8 is removed to expose the lower side of the leadframe. A solder paste is screen printed or dispensed for copper studded MOSFETs that are flip chip attached to leadframes. The solder paste is screen printed onto the lower side of the leadframe. It is patterned to define the solder connections for the MOSFETs to the leadframe and the solder ball connections for the outer leads. Ball contacts are applied to the outer leads on the lower surface of the lead frame. Selected leads on the upper side are wire bonded to the controller integrated circuit.

The assembled multichip module 30 is shown in FIG. 17. The upper surface of the central die pad has a die attach epoxy 12 that holds the integrated circuit controller 14 to

the central die pad. Wire bonds 16 extend from contact areas on the integrated circuit to outer leads 2.6 of the lead frame 10. The integrated circuit is encapsulated in an insulating plastic resin 18. On the opposite, lower side of the central die pad, the MOSFETs 50, 60 are bump or stud attached to the half etched regions of the lead frame. The bumps or studs 22.2 are preferably copper stud bumps. The half etched leadframe provides connections to the outer leads for the MOSFETs. The drains 37 of the MOSFETs and the ball contacts 22.1 on the outer leads are soldered to a printed circuit board.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues are whether Claims 1, 3, and 4 are patentable under 35 U.S.C 103(a) over Joshi combined with Huang; whether Claim 2 is patentable under 35 U.S.C. 103(a) over Joshi combined with Huang, and in further view of Estacio; whether Claims 5, 6, and 9 – 15 are patentable under 35 U.S.C. 103(a) over Joshi combined with Huang and Woodworth.

ARGUMENT

In the Office Action mailed October 5, 2005, claims 1, 3, and 4 were rejected under 35 U.S.C. § 103 (a) based upon a combination of U.S. Patent No. 6,798,044 (Joshi) and a published U.S. application U.S. 2002/0113305 (Huang). Claim 2 was rejected based upon those two combined with U.S. 2003/089248 (Estacio). Claims 5, 6, and 9 – 15 were rejected based upon those two combined with U.S. 6,476,481 (Woodworth et al).

Claims 1, 3, and 4 are Patentable Over Joshi in view of Huang

Responsive to the Examiner's rejection of Claims 1, 3, and 4 under 35 U.S.C. 103(a) as being unpatentable over Joshi in view of Huang, Appellant respectfully submits that the Examiner has not established a *prima facie* case of obviousness. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Moreover, obviousness can only be established by combining or modifying the teachings of the prior art where there is some teaching, suggestion, or motivation to do so found in either the references themselves or in the knowledge generally available to one of the ordinary skill in the art. *In re Fine,* 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones,* 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). The present invention is neither taught nor suggested by Joshi combined with Huang. As a result, a *prima facie* case of obviousness has not been established.

The Examiner states that it would have been obvious to one of ordinary skill in the art to modify the MOSFET device of Joshi to include a die pad and connections using outer leads and bonding wires as discussed in Huang. The Appellant points out that the Examiner has not cited any section of either Joshi or Huang as providing the suggestion or motivation necessary for rendering such a combination *prima facie* obvious.

Joshi teaches **one** technique – flip chip mounting – for connecting two dies to a lead frame. Specifically, Joshi provides "a chip device that includes two dies stacked atop one another. The use of solder bumps allows for a small package profile," column 1,

lines 42 - 44. Joshi does not teach using different mounting connections for each die. Nor does Joshi teach connecting a die via wire bonding.

In contrast, Independent Claim 1 of the present invention includes the limitation of "an integrated circuit mounted on the upper surface of the die pad and **having contact areas for receiving bond wires; bond wires extending from the contact areas on the integrated circuit to the outer leads of the leadframe**; one or more power mosfet semiconductor devices flip chip mounted on the lower surface of the leadframe." The claims are distinctive from Joshi because the language "having contact areas for receiving bond wires" indicates that each of the two dies are mounted using **different** techniques, for different dies in one module (wire bonding for one and flip chip for another), while Joshi teaches the **same** technique (flip chip) in one module for mounting **both** dies.

The present claims are directed to an invention that has the advantage of being a multi-chip package with flip chip features and a wire bonded fully encapsulated device, whereas Joshi is limited to flip chip mounted device, as stated by Joshi in lines 9 and 10 of column 3. As a result, Joshi requires that surfaces be exposed on both dies on both sides of the package. Huang, teaching a fully encapsulated package wherein both dies are wire bonded, does not overcome these deficiencies. Wire bonded dies are fully encapsulated, have no exposed surface, and - prior to the present invention - were considered incompatible with flip chip packaging.

A prima facie case of obviousness may be rebutted by showing that the art, in any material respect, teaches away from the claimed invention. *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997). It is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983).

Joshi explicitly teaches away from wire bonding as a method for attaching the dies. Joshi states, "**the non-use of wire bond interconnect** allows for accommodating a very large size die for a given molded package body outline," column 1, lines 44 – 49 (emphasis added), and "**the non-use of wire bond interconnect** allows for accommodating a very large size die for a given molded package," column 3, lines 9 – 11 (emphasis added). In contrast, Claim 1 of the present invention explicitly employs a wire bonding technique as discussed above.

Like Joshi, Huang also teaches away from the present invention. Specifically, Huang teaches away from: (1) flip chip mounting; and (2) mounting both dies on a **single** lead frame using a **single** die pad. Huang requires two lead frames, each with its own die pad. Huang claims "a first leadframe having a die pad...a second leadframe having a die pad..." paragraphs [0047] – [0048]. The use of two lead frames and two die pads is central to Huang's invention. He suggests that flip-chip mounting two dies to only one lead frame and one die pad may result in the two dies becoming "damaged," "imprecisely aligned," "deformed," or "delaminated," paragraphs [0016] – [0022]. In contrast, Independent Claim 1 of the present invention is directed toward "one lead frame," and is limited to a single lead frame and a single die pad.

There is no suggestion to combine Joshi and Huang. If one followed Huang and combined Huang and Joshi, one would use **two** die pads and **two** lead frames. Moreover, one skilled in the art would be led to selecting **either** wire bonding or flip chip mounting for **both** dies, as Joshi teaches away from wire bonding and Huang teaches away from flip-chip mounting. The Examiner has not pointed out any suggestion in Joshi or Huang to combine both wire bonding and flip chip mounting on a single dual-die device. There is no disclosure in either reference to mix connection types.

Claim 2 is Patentable over Joshi in view of Huang and Estacio

Responsive to the Examiner's rejection of Claim 2 under 35 U.S.C. 103(a) as being unpatentable over Joshi in view of Huang and Estacio, Appellant respectfully submits that the Examiner has not established a *prima facie* case of obviousness. The Examiner correctly points out neither Joshi nor Huang recite source bump contacts in the surface of the MOSFETs and the gate bump contacts extending to a corresponding outer lead. As discussed above, there is no suggestion to combine Joshi with Huang. In addition, there is no suggestion to combine these references with Estacio to overcome these deficiencies.

Joshi and Huang are directed toward dual-die stacked devices. Estacio is directed toward a method for creating "dual or multiple gate pads for a single gate contact" on a single MOSFET die, paragraph [0018]. Particularly, Estacio is directed toward a method

for extending "under-bump metal laterally from the gate contact with the gate pad metallization out to **two or more gate pads** not overlying the gate pad metallization," paragraph [0007] (emphasis added). Joshi teaches a "single, common lead frame," and a first and second "bumped die" flipped and soldered to the lead frame, column 3, lines 17 - 25. Joshi does not teach source bump contacts in the surface of the MOSFETs, and the gate bump contacts extending to a corresponding outer lead. Huang teaches a dual-die integrated circuit package employing a wire bond process. The Examiner has failed to point out a suggestion in Estacio to combine his invention with one that employs wire bond interconnects, or one for creating a dual-die stacked device incorporating multiple connection types.

Claims 5, 6, and 9 – 15 are Patentable over Joshi in view of Huang and Woodworth

Responsive to the Examiner's rejection of Claims 5, 6, and 9 - 15 under 35 U.S.C. 103(a) as being unpatentable over Joshi in view of Huang and Woodworth, Appellant respectfully submits that the Examiner has not established a *prima facie* case of obviousness. The Examiner correctly points out Joshi does not suggest the following elements found in the present invention: (1) source bump contacts in the surface of the MOSFETs and gate bump contacts extending to a corresponding outer lead; (2) die pad terminology; (3) bonding wires; nor (4) different connections from ball grid or stud grid. Huang does not suggest using a single lead frame and die pad nor flip chip mounting. It is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983). As discussed above, Joshi explicitly teaches away from wire bonding connections. Similarly, Huang explicitly teaches away from flip-chip mounting, as well as the use of a single lead frame and a single die pad. These elements are also found in the present invention.

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP

Section 2143.01 III. The Examiner has pointed out no suggestion to combine these references with Woodworth to overcome these deficiencies.

Woodworth teaches a semiconductor with a single die, a plurality of bonding wires, a die mounting pad, and a plurality of external conductors reentrantly bent and penetrating a side wall of a plastic housing (column 7, lines 1-17). Woodworth simply does not teach a dual-die structure, nor a dual-die structure with a ball array or stud array connection.

For all the foregoing reasons, Appellant submits that the pending claims are in condition for allowance, hereby respectfully requested.

Respectfully submitted,

HISCOCK & BARCLAY, LLP

By: _____

Thomas R. Fitzgerald
Reg. No. 26,730
2000 HSBC Plaza
Rochester, NY 14604
Tel: (585) 295-4469
Fax: (585) 295-5458

CLAIMS APPENDIX

Claim 1. A multi flip chip module comprising:

a leadframe having a die pad with upper and lower surfaces and a plurality of outer leads surrounding the die pad;

an integrated circuit mounted on the upper surface of the die pad and having contact areas for receiving bond wires;

bond wires extending from the contact areas on the integrated circuit to the outer leads of the leadframe;

one or more power mosfet semiconductor devices flip chip mounted on the lower surface of the leadframe; and

a molded resin encapsulating the integrated circuit and leaving exposed at least one surface of the power mosfet semiconductor devices.

Claim 2. The multichip module of claim 1 wherein the mosfets have source bump contacts extending from the surfaces of the mosfets to the die pad and one or more gate bump contacts for each mosfet extending to a corresponding outer lead.

Claim 3. The multichip module of claim 1 wherein the lead frame has leadless contacts comprising ball contacts extending from the outer leads for establishing an electrical connection to the contact areas of the integrated circuit via the bond wires and for providing surface mounts for connecting the semiconductor device to a surface of an electrical component board.

Claim 4. The multichip module of claim 1 wherein exposed surface(s) of the power mosfets are surface mountable on an electrical component board.

Claim 5. A multichip module having a lead frame with a central die pad and peripheral outer leads, an integrated circuit on one side of the die pad, wire bonds for connecting the integrated circuit to outer leads, one or more mosfets having their respective source and gate bumps connected to the other side of the central die pad, said central die pad patterned to provide connections to the outer leads from the source and gate bump connections.

Claim 6. The multichip module of claim 5 wherein the integrated circuit is encapsulated in an insulating resin.

Claim 7 – 8. Cancelled.

Claim 9. A multi flip chip module comprising:

a leadframe having a die pad with upper and lower surfaces and a plurality of leads surrounding the die pad;

an integrated circuit mounted on the upper surface of the die pad and having contact areas for receiving connections to the outer leads;

a first type of electrical and mechanical connection for connecting terminals of the integrated circuit to the outer leads of the leadframe;

one or more power mosfet semiconductor devices mounted on the lower surface of the leadframe; and

a second type of electrical and mechanical connection, different from the first type, for connecting the power mosfet(s) to the leadframe; and

a molded resin encapsulating the integrated circuit and leaving exposed at least one surface of the power mosfet semiconductor devices.

Claim 10. The multi flip chip module of claim 9 wherein the second type of electrical connection is a bond wire connection.

Claim 11. The multi flip chip module of claim 9 wherein the second type of electrical connection is a ball array or stud array connection.

Claim 12. A multi flip chip module comprising:

a leadframe having a die pad with upper and lower surfaces and a plurality of outer leads surrounding the die pad;

an integrated circuit mounted on the upper surface of the die pad and having contact areas for receiving connections to the outer leads;

wire bonds connecting contact areas of the integrated circuit to the leads of the leadframe;

one or more power mosfet semiconductor devices mounted on the lower surface of the leadframe; and

an electrical and mechanical connection different from wire bonds for connecting the power mosfet(s) to the leadframe; and

a molded resin encapsulating the integrated circuit and leaving exposed at least one surface of the power mosfet semiconductor devices.

Claim 13. The multi flip chip package of claim 12 wherein the electrical and mechanical connection different from wire bonds for connecting the power mosfet(s) to the leadframe comprises a ball grid array or a stud grid array.

Claim 14. A multi flip chip module comprising:

a leadframe having a die pad with upper and lower surfaces and a plurality of outer leads surrounding the die pad;

an integrated circuit mounted on the upper surface of the die pad and having contact areas for receiving connections to the outer leads;

an electrical and mechanical connection different from ball grid or stud grid array for connecting contact areas of the integrated circuit to the leads of the leadframe;

one or more power mosfet semiconductor devices mounted on the lower surface of the leadframe; and

ball grid or stud grid arrays for connecting the power mosfet(s) to the leadframe; and

a molded resin encapsulating the integrated circuit and leaving exposed at least one surface of the power mosfet semiconductor devices.

Claim 15. The multi flip chip package of claim 12 wherein the electrical and mechanical connection different from ball grid array or stud grid array is a wire bond connection.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.

$AR 1/FW

PTO/SB/21 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

Application Number	10/803,464
Filing Date	March 18, 2004
First Named Inventor	Jonathan A. Noquil
Art Unit	2826
Examiner Name	Tuan Quach
Attorney Docket Number	3016271(67130)

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) ____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below)*:
  Acknowledgement Postcard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm	Hiscock & Barclay LLP		
Signature	Thomas R. FitzGerald		
Printed Name	Thomas R. FitzGerald		
Date	April 28, 2006	Reg. No.	26,730

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Signature	Kathleen A. Manczuk		
Typed or printed name	Kathleen A. Manczuk	Date	April 28, 2006

PTO/SB/92 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Certificate of Mailing under 37 CFR 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:

Commissioner for Patents
Mail Stop: Appeal Brief - Patents
P.O. Box 1450
Alexandria, VA 22313-1450

on April 28, 2006
Date

Kathleen A. Manczuk
Signature

Kathleen A. Manczuk
Typed or printed name of person signing Certificate

Registration Number, if applicable

585-325-7570
Telephone Number

Note: Each paper must have its own certificate of mailing, or this certificate must identify each submitted paper.

Appeal Brief (17 pages)

PTO/SB/17 (01-06)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

*Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL for FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($) 500.00

Complete if Known	
Application Number	10/803,464
Filing Date	March 18, 2004
First Named Inventor	Jonathan A. Noquil
Examiner Name	Tuan Quach
Art Unit	2826
Attorney Docket No.	3016271 (67130)

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify) : _____

☑ Deposit Account Deposit Account Number: 50-3010 Deposit Account Name: Hiscock & Barclay, LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☑ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☐ Charge any additional fee(s) or underpayments of fee(s) Under 37 CFR 1.16 and 1.17 ☐ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee($)	Fee($)	Fee($)	Fee($)	Fee($)	Fees Paid ($)
Utility	300	150	500	250	200	100	____
Design	200	100	100	50	130	65	____
Plant	200	100	300	150	160	80	____
Reissue	300	150	500	250	600	300	____
Provisional	200	100	0	0	0	0	____

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims		Fee($)		Fee Paid ($)
____	-20 or HP=	____	x	____	=	____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		Extra Claims		Fee($)		Fee Paid ($)
____	- 3 or HP=	____	x	____	=	____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
____	____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof		Fee ($)		Fee Paid ($)
____	- 100 =	____	/ 50 =	____	(round up to a whole number) x	____	=	____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	____
Other (e.g., late filing surcharge) : Appeal Brief	500.00

SUBMITTED BY

Signature	Thomas R. FitzGerald	Registration No. (Attorney/Agent) 26,730	Telephone 585-325-7570
Name (Print/Type)	Thomas R. FitzGerald		Date April 28, 2006